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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,593	03/09/2001	Matthew S. Blaha	BLAHA 2	8188

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EXAMINER

PATHAK, SUDHANSHU C

ART UNIT PAPER NUMBER

2611

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/803,593	Applicant(s) BLAHA, MATTHEW S.	
	Examiner Sudhanshu C. Pathak	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on May 22nd, 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on March 9th, 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-to-20 are pending in the application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-2, 4-6, 7-9, 11-13, 14-16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Sevic et al. (5,872,481) in further view of Sampei et al. (3,961,280).

Regarding to Claims 1, 4, 7-8, 11 & 14, the Applicant Admitted Prior Art (AAPA) discloses a line driver couplable to a transmission path having line characteristics associated therewith, comprising: a driver stage configured to send a signal along said transmission path (Specification, Page 1, Paragraph 2). The AAPA also discloses the power necessary to drive a signal down a transmission medium depending on the line characteristics (Specification, Page 2, Paragraph 3). However, the AAPA does not disclose a switching network, coupled to the driver configured to adaptively select a power level to send a signal down a transmission medium as a function of line characteristics of the transmission path.

Sevic discloses a power amplifier comprising a plurality of amplifiers configured to amplify the signal to be transmitted (Abstract, lines 1-13 & Fig. 2, elements A1-A4 & Fig. 5A-B). Sevic further discloses a switching network comprising a plurality of switches configured to couple the driver to ground (Fig. 2, element 56 & Fig. 5A-B, element 56, 74-84 & Fig. 11, elements 1120, 1102-1108 & Column 7, lines 55-67 & Column 8, lines 1-67 & Column 9, lines 1-67 & Column 10, lines 1-5). Sevic also discloses the selecting, by the control circuit, the appropriate amplifier stage in response to a desired power value (Abstract, lines 1-10). Sevic further discloses the desired power level is a minimum power level necessary to maintain quality communications (Column 2, lines 4-7). Sevic also discloses determining channel conditions to further determine the desired power level for transmission of the signal through the channel (Column 1, lines 49-67 & Column 2, lines 3-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sevic teaches a switching network coupled to an amplifier so as to select an appropriate amplifier stage to achieve a desired power level for transmission, and further Sevic also teaches determining channel conditions to determine the desired power level, and this can be implemented in the DSL driver as described in the AAPA so as to adaptively select the power level to send a signal as a function of transmission line characteristics, thus satisfying the limitations of the claim. However, AAPA in view of Sevic does not disclose the switching network to select a voltage level to apply across the driver stage to provide a power level to the amplifier stage.

Sampei discloses an amplifier circuit comprising an amplifying transistor and a switching transistor (Abstract, lines 1-13 & Fig. 1, elements 5-6). Sampei further discloses the switching transistor to be a switching circuit for providing (selectively connecting) from a multiple of different power (supplies i.e. voltages) to the amplifying transistor in response to a control signal (Abstract, lines 1-13 & Column 1, lines 65-68 & Column 2, lines 1-6, 50-68 & Column 3, lines 1-26, 54-68 & Column 4, lines 1-11 & Fig. 1, elements 5-6, 8-9 & Fig. 3, elements 5-6, 17-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sampei teaches implementing a switching circuit to selectively connect and disconnect a power supply (from a multiple of different power supplies) to an amplification stage and this can be implemented in the DSL driver as described in the AAPA in view of Sevic so as to provide the amplifier with increased output power (gain), without the distortion due to the saturation of the amplifier (stage).

Regarding to Claims 2 & 9, the Applicant Admitted Prior Art (AAPA) in view of Sevic in further view of Sampei discloses a line driver amplifier comprising a driver stage configured to send a signal along the transmission path, and a switching network coupled to the driver stage, configured to adaptively select a voltage level to apply across the driver stage to provide a power level of the transmitted signal as a function of the line characteristics described above. Sevic also discloses a power amplifier comprising a plurality of amplifiers configured to amplify the signal to be transmitted (Abstract, lines 1-13 & Fig. 2, elements A1-A4 & Fig. 5A-B). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention

that Sevic teaches implementing a power amplifier as a combination of plurality of individual amplifiers and this can be implemented as the driver stage of the line driver amplifier as described in AAPA in view of Sevic in further view of Sampei so as to vary the transmitted power of the driver amplifier and improving the efficiency of the line driver amplifier depending on the transmission path characteristics, thus satisfying the limitation of the claim.

Regarding to Claims 5, 12 & 19, the Applicant Admitted Prior Art (AAPA) in view of Sevic in further view of Sampei discloses a line driver amplifier comprising a driver stage configured to send a signal along the transmission path, and a switching network coupled to the driver stage, configured to adaptively select a voltage level to apply across the driver stage to provide a power level of the transmitted signal as a function of the line characteristics described above. Sevic further discloses a power amplifier comprising a plurality of amplifiers configured to amplify the signal to be transmitted (Abstract, lines 1-13 & Fig. 2, elements A1-A4 & Fig. 5A-B). Sevic further discloses a switching network comprising a plurality of switches configured to couple the driver to ground (Fig. 2, element 56 & Fig. 5A-B, element 56, 74-84 & Column 7, lines 55-67 & Column 8, lines 1-67 & Column 9, lines 1-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the switching network as described in Sevic can be implemented as a driver stage as described in the AAPA in view of Sevic in further view of Sampei so as to vary the power transmitted depending on the desired user, thus satisfying the limitations of the claim.

Regarding to Claims 6, 13 & 20, the Applicant Admitted Prior Art (AAPA) in view of Sevic in further view of Sampei discloses a line driver amplifier comprising a driver stage configured to send a signal along the transmission path, and a switching network coupled to the driver stage, configured to adaptively select a voltage level to apply across the driver stage to provide a power level of the transmitted signal as a function of the line characteristics described above. Sampei further discloses the power levels to transmit the signal depending on the supply voltage levels, and the supply voltage is arbitrarily set depending on the circuit components and applications (Fig. 1, elements 8-9 & Fig. 3, elements 19-21 & Column 2, lines 40-68 & Column 3, lines 1-68 & Column 4, lines 1-24). Sampei further discloses a push-pull amplifier configuration for balancing the positive and negative polarity for the input / output waveforms (Fig. 9, Column 6, lines 25-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sampei teaches that the maximum transmit power level voltage depends on the supply voltage levels of the amplifier circuit and this driver configuration can be implemented in the line driver as described in the AAPA in view of Sevic so as to set the maximum output power level voltage of the driver. Furthermore, even though Sampei does not specify a power level up to about 21 volts, there is no criticality in configuring the line driver power level up to the 21 volts, and this is only a matter of design choice.

Regarding to Claims 15 & 18, the Applicant Admitted Prior Art (AAPA) discloses a line driver couplable to a transmission path having line characteristics associated

therewith, comprising: a driver stage configured to send a signal along said transmission path (Specification, Page 1, Paragraph 2). The AAPA also discloses the power necessary to drive a signal down a transmission medium depending on the line characteristics (Specification, Page 2, Paragraph 3). However, the AAPA does not disclose a switching network, coupled to the driver configured to adaptively select a power level to send a signal down a transmission medium as a function of line characteristics of the transmission path.

Sevic discloses a power amplifier comprising a plurality of amplifiers configured to amplify the signal to be transmitted (Abstract, lines 1-13 & Fig. 2, elements A1-A4 & Fig. 5A-B). Sevic further discloses a switching network comprising a plurality of switches configured to couple the driver to ground (Fig. 2, element 56 & Fig. 5A-B, element 56, 74-84 & Fig. 11, elements 1120, 1102-1108 & Column 7, lines 55-67 & Column 8, lines 1-67 & Column 9, lines 1-67 & Column 10, lines 1-5). Sevic also discloses the selecting, by the control circuit, the appropriate amplifier stage in response to a desired power value (Abstract, lines 6-10). Sevic further discloses the desired power level is a minimum power level necessary to maintain quality communications (Column 2, lines 4-7). Sevic also discloses determining channel conditions to further determine the desired power level for transmission of the signal through the channel (Column 1, lines 49-67 & Column 2, lines 3-19). Sevic discloses a transceiver comprising a power amplifier for driving a signal to the transmission path (Fig. 6 & Fig. 7) further comprising a conversion stage that converts signals between an analog and digital domain (Fig. 7, elements 270, 272);

and a filter stage, coupled to said conversion stage, that filters the signals (Fig. 7, elements 264, 266). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sevic teaches a switching network coupled to an amplifier so as to select an appropriate amplifier stage to achieve a desired power level for transmission, and further Sevic also teaches measuring channel conditions to determine the desired power level. Sevic also teaches implementing the line driver in a transceiver and processing the data to be transmitted so as to be compatible to the driver as described in the AAPA for transmission over the transmission path, and this can be implemented in the DSL driver as described in the AAPA so as to adaptively select the power level to send a signal as a function of transmission line characteristics, thus satisfying the limitations of the claim.

However, AAPA in view of Sevic does not disclose the switching network to select a voltage level to apply across the driver stage to provide a power level to the amplifier stage.

Sampei discloses an amplifier circuit comprising an amplifying transistor and a switching transistor (Abstract, lines 1-13 & Fig. 1, elements 5-6). Sampei further discloses the switching transistor to be a switching circuit for providing (selectively connecting) from a multiple of different power (supplies i.e. voltages) to the amplifying transistor in response to a control signal (Abstract, lines 1-13 & Column 1, lines 65-68 & Column 2, lines 1-6, 50-68 & Column 3, lines 1-26, 54-68 & Column 4, lines 1-11 & Fig. 1, elements 5-6, 8-9 & Fig. 3, elements 5-6, 17-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention

that Sampei teaches implementing a switching circuit to selectively connect and disconnect a power supply (from a multiple of different power supplies) to an amplification stage and this can be implemented in the DSL driver as described in the AAPA in view of Sevic so as to provide the amplifier with increased output power (gain), without the distortion due to the saturation of the amplifier (stage).

Regarding to Claim 16, the Applicant Admitted Prior Art (AAPA) in view of Sevic in further view of Sampei discloses a line driver amplifier comprising a driver stage configured to send a signal along the transmission path, and a switching network coupled to the driver stage, configured to adaptively select a voltage level to apply across the driver stage to provide a power level of the transmitted signal as a function of the line characteristics described above. Sevic also discloses a power amplifier comprising a plurality of amplifiers configured to amplify the signal to be transmitted (Abstract, lines 1-13 & Fig. 2, elements A1-A4 & Fig. 5A-B). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sevic teaches implementing a power amplifier as a combination of plurality of individual amplifiers and this can be implemented as the driver stage of the line driver amplifier as described in AAPA in view of Sevic in further view of Sampei so as to vary the transmitted power of the driver amplifier and improving the efficiency of the line driver amplifier depending on the transmission path characteristics, thus satisfying the limitation of the claim.

5. Claims 3, 10 & 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Sevic et al. (5,872,481) in further view of Sampei (3,961,280) in further view of Lee (3,755,693).

Regarding to Claims 3, 10 & 17, the Applicant Admitted Prior Art (AAPA) in view of Sevic in further view of Sampei discloses a line driver amplifier comprising a driver stage, comprising a plurality of amplifiers, configured to send a signal along the transmission path, and a switching network coupled to the driver stage, configured to adaptively select a voltage level to apply across the driver stage to provide a power level of the transmitted signal as a function of the line characteristics described above. However, the references do not disclose the driver stage further comprising a reference circuit configured to provide a reference level.

Lee discloses a voltage reference circuit configured to provide a voltage reference level associated with the corresponding circuitry (Column 1, lines 1-40 & Column 2, lines 1-27 & Fig. 1, elements 2, 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Lee discloses an interface circuitry that can be implemented in the line driver as described in the AAPA in view of Sevic in further view of Sampei so as to avoid incompatibility (saturation) between the voltage swing level of the input signal and the switching (varying) supply voltage of the driver circuitry, thus satisfying the limitation of the claim.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

- If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571)-272-3042
- The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.
- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER